Bryan Guner 9/26/16

Homework#1

#2:

ro=0x0f0f0f0f

r1=0xFEDCBA98

(1)EOR r3,r1,r0: F1D3B597

(2)ORR r3,r1,r0: FFDFBF9F

(3)AND r3,r1,r0: E0C0A08

(8)MVN r3,r0: 1EFCEAB88

ADD r3,r1,r3

#4.

SMULr3,r0,r1

ADD r3,r3,r2

SUB r3,r3,r0

#6.

SMUL r3,r0,r0

SMUL r4,r3,r0

ADD r5,r4,r4

ADD r6,r5,r4

ADD r7,r4,r4

ADD r7,r7,r4

ADD r7,r7,r4

ADD r7,r7,r4

ADD r7,r7,r4

ADD r7,r7,r4

ADD r8,r0,r0

ADD r8,r8,r0

ADD r8,r8,r0

ADD r8,r8,r0

ADD r8,r8,r0

ADD r8,r8,r0

ADD r8,r8,r0

ADD r8,r8,r0

ADD r8,r8,r0

SUB r3,r6,r7

ADD r3,r3,r8

SUBI r1,r3,11

#8. Cortex M-3 processors do not provide any rotation left instructions because they can be preformed using rotation right instructions. N-bit rotation to the left equals 32-n rotations to the right.

#7

1. let r1=1010101010101010

AND r2,r0,r1

(2)let r1=0101010101010101

ORR r2,r0,r1

(3)let r1=1010101010101010

EOR r2,r0,r1